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Large scale 3D vertical assembly of single-wall carbon nanotubes at ambient temperatures

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Abstract

We demonstrate three-dimensional directed assembly of single-wall carbon nanotubes (SWNT) into porous alumina nanotemplates on silicon substrates by means of electrophoresis and dielectrophoresis at ambient temperatures. Assembled SWNT provided an interconnection between the surface and base of the nanotemplate. I–V measurements clearly show that the connection between silicon and SWNT is established inside the templates. This technique is particularly useful for large scale, rapid, 3D assembly of SWNT over centimeter square areas under mild conditions for nanoscale electronics applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

After recent discoveries regarding their electronic properties like large current capacities as high as 10^9 A cm^{-2} [1] or mobility as high as 100 000 cm^2 V^{-1} s^{-2} [2], single-wall carbon nanotubes (SWNT) have become one of the most popular structures in nanoscale electronics. They have tremendous importance especially as electrical interconnects since current materials (e.g. copper wires) fail to meet the required resistivity for smaller diameters [3].

A key challenge in utilizing carbon nanotubes (CNT) in nanoscale electronics is to assemble them for large scale device applications. Presently there are two main approaches for manufacturing CNT: growing or assembling them into the device. All the various methods for growing CNT require high temperature synthesis [4, 5] and in most of them, nanotubes need a post process for cleaning, cutting and sorting to reach a narrow size distribution as well as for purification to eliminate the impurities which depends on the synthesis technique [6].

In contrast to methods for growing CNT, post-synthesis assembly methods permit arranging nanotubes in a desired position without the need for high temperatures. With assembly methods, we have the flexibility to choose and use any SWNT solution (e.g. commercially available) for desired applications. Many different assembly methods such as transfer printing [7], surface-functionalization [8], magnetic field assisted [9] and electric field assisted assembly [10–14] have been investigated so far. A key challenge in utilizing CNT in nanoscale electronics is the assembly of the CNT for large scale devices. For devices such as electronic memories, assembly of the nanoelements needs to be done over millimeter square areas.

In this paper we present a method to assemble SWNT into anodic aluminum oxide (AAO) nanotemplates utilizing electric field assisted assembly [15]. Nanoporous alumina templates consist of an array of vertically arranged nano-sized cylindrical holes and provide a useful platform for the development of a variety of novel nanofabrication techniques [16, 17].

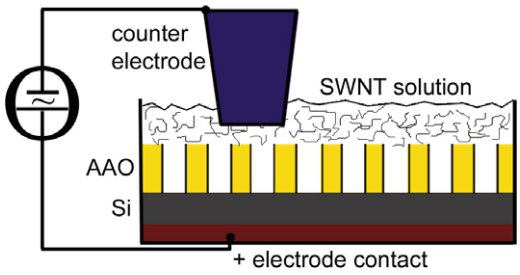

Figure 1. Schematic of CNT assembly. The positive electrode is attached to the Si substrate under alumina template while a Pt–Ir wire is used as counter electrode.

They also have been used in high temperature synthesis of ordered CNT arrays [18–21]. Here, we utilize AAO's high-rate scalability over centimeter square areas to demonstrate a post-synthesis assembly method rather than growing SWNT to avoid high temperature synthesizing conditions. The assembly was performed on a silicon (Si) substrate, enabling seamless integration into today's semiconductor electronics industry.

2. Experimental details

2.1. Fabrication of nanotemplates

Porous alumina nanotemplates were prepared on 0.1 × 0.1 cm^2 n-doped silicon (Si) substrates (3–7 Ω cm resistivity). 1 μm thick aluminum (Al) was deposited by electron beam deposition on Si. The base pressure was 2×10^{-7} Torr and deposition rate was kept at 5 Å s^{-1}. Nanoporous alumina templates were prepared by anodization [22, 23] of Al surface on the Si chip in 5 wt% oxalic acid. Anodization was carried out at 5 °C under a constant 40 V DC potential until the whole Al layer was consumed (which took approximately 12 min). This one-step anodization procedure produces a nanoporous layer with a barrier layer of aluminum oxide on the Si surface. The barrier layer was removed by soaking in 5 wt% phosphoric acid for 40 min. The total area of alumina array is 0.4 cm^2 and with pore diameter of the order of 40 nm and thickness of the order of 1 μm.

2.2. Assembly of SWNT

Negatively charged SWNT (Nantero, MA) are used for assembly. The SWNT solution was prepared in ethanol and assembly occurred under 10 V DC together with 10 V AC at 10 MHz. The positive electrode was attached to the bottom of the template (Si) while the negative electrode is connected to a Pt–Ir wire. The schematic of the assembly is illustrated in figure 1. The position of the counter electrode was swept manually along the x–y plane such that it covered approximately 50 different assembly sites on the surface of AAO. The purpose of raster scanning of the counter electrode was to expand the assembly coverage over the entire surface, which is 0.32 cm^2. A control experiment of AAO immersed in SWNT solution was conducted without applying an electric field to further investigate the effect of applied field on assembly.

2.3. I–V measurement

After assembly, a 15 nm thick Au layer was sputtered on 0.015 cm^2 area of alumina template surface by a sputter coater to make an electric connection between all the SWNT on the surface. The I–V measurement was done using a parameter analyzer attached to a probe station by connecting one electrode on Au layer on the surface of alumina and the other on Si surface at the bottom of the template. As control measurement, I–V curve was measured using the same AAO templates on Si substrate covered by Au layer without assembled SWNT (figure 2).

3. Results and discussion

For electric field assisted assembly of SWNT, a wire shaped counter electrode was used instead of parallel plate electrodes. The main reason of using a pointed counter electrode is that the distance between the electrodes can be arranged more precisely in this way. The counter electrode can be approached much closer and the resulting electric field magnitude consequently is larger.

The non-uniformity of the electric field is another reason of choosing pointed electrode. The total force acting on a charged particle in the solution is the sum of electrophoretic and dielectrophoretic forces, $\mathbf{F} = \mathbf{F}_{\mathrm{EP}} + \mathbf{F}_{\mathrm{DEP}}$. Electrophoretic force acting on a charged particle is $\mathbf{F}_{\mathrm{EP}} = \Gamma \varepsilon_{\mathrm{m}} \zeta \mathbf{E}$ where Γ is geometry factor, ε_{m} relative permittivity of medium and ζ is the zeta-potential of particle. The dielectrophoretic force acting on a dielectric particle can be calculated as $\mathbf{F}_{\mathrm{DEP}} = \Lambda \varepsilon_{\mathrm{p}} \mathrm{Re}\{\kappa_f(\omega)\} |\mathbf{E}| \nabla |\mathbf{E}|$, where Λ the factor depends on the geometry, ε_{p} relative permittivity of particle and κ_f is Clausius–Mossotti factor depending both on geometry and frequency.

If SWNT are considered ellipsoid in shape, the electrophoretic force would not differ much from the spherical calculation except from the geometry factor, Γ. However, dielectrophoretic force might change a lot depending Clausius–Mossotti factor, κ_f [24]. κ_f for an ellipsoid particle with a cylindrical symmetry could be written as $\kappa_f = \mathrm{Re}\{(\varepsilon_{\mathrm{p}}^* - \varepsilon_{\mathrm{m}}^*)/3[(\varepsilon_{\mathrm{p}}^* - \varepsilon_{\mathrm{m}}^*)A + \varepsilon_{\mathrm{m}}^*]\}$, where $\varepsilon_{\mathrm{p}}^*$ and $\varepsilon_{\mathrm{m}}^*$ are the complex permittivity of particle and medium respectively and A is the depolarizing factor given by $A = (1 - e^2)/2e^3[\ln((1 + e)/(1 - e)) - 2e]$. e defined as $e \equiv \sqrt{1 - (b/a)^2}$, where a and b are the major and minor axis of ellipsoid respectively [25].

For successful assembly, it is necessary to avoid the charged nanotubes sticking on the positive electrode surface of AAO. For this reason an AC electric field is used together with DC field. The AC field does not contribute to the electrophoretic force and hence does not cause the nanotubes to move directly towards the alumina surface. However, it helps the nanotubes to orient and to move into the holes by dielectrophoretic force.

We used $2.5\varepsilon_0$ and 10^5 S m^{-1} for semiconducting nanotubes (s-SWNT) and $-10^4\varepsilon_0$ and 10^8 S m^{-1} for metallic ones (m-SWNT) as the values of permittivity and conductivity respectively [9]. ε and σ for ethanol is taken as $25\varepsilon_0$ and 6 μS m^{-1}. By using these values Clausius–Mossotti factor

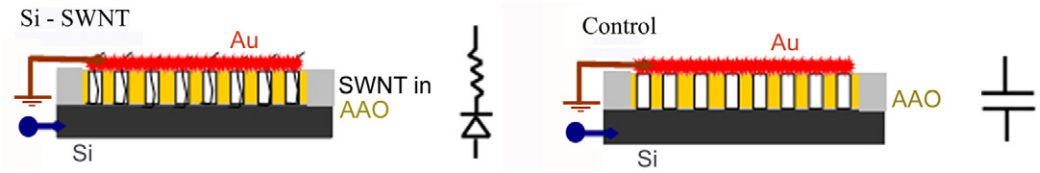

Figure 2. Schematic of I–V measurement of SWNT assembly and control.

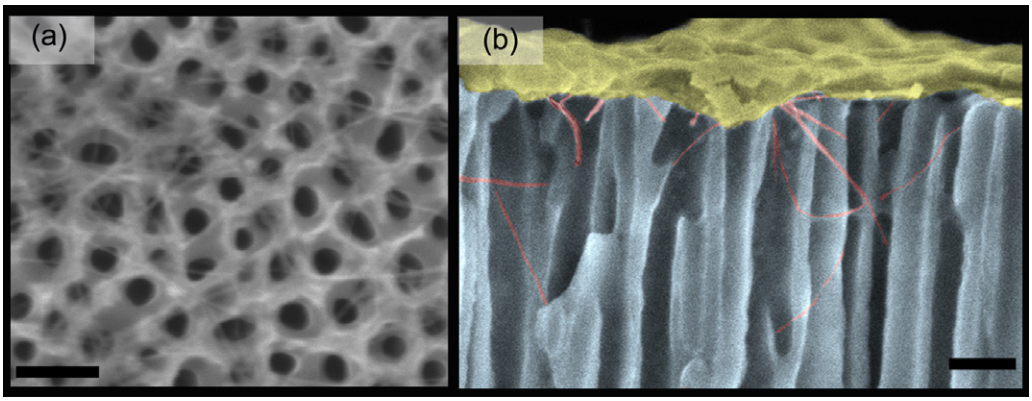

Figure 3. SEM micrographs of assembled SWNT in anodic alumina array: (a) top view and (b) cross-sectional view. The top layer at this false colored picture is the sputtered Au for imaging purposes. The scale bars are 120 nm.

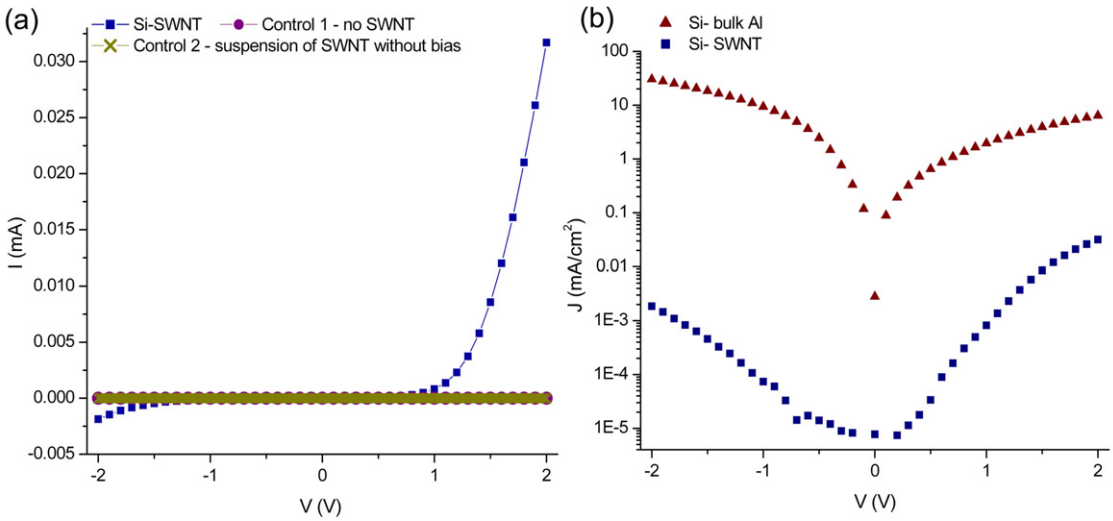

Figure 4. (a) I–V measurements curves for different connections. The blue (square) data set is the connection between SWNT–Si. The purple (circle) data set is the first control experiment with the absence of nanotube and the green (cross) data set is the second control experiment with SWNT suspension on AAO but without bias. No current is observed in the absence of either SWNT or the applied electrical field for the assembly. (b) Current density–voltage characteristics of Si-bulk Al and Si–SWNT connections. The current density of SWNT connection is calculated over the total measurement area.

was estimated as $\kappa_f^{\mathrm{s-SWNT}} = -0.3$ and $\kappa_f^{\mathrm{m-SWNT}} = -134$ for electric field parallel to the major axis of nanotubes under DC field or low frequencies (including 10 MHz which we are working in). These calculations show that actually metallic and semiconducting tubes are moving in the same direction but the force on metallic nanotubes is 400 times larger than the semiconducting ones.

The size of SWNT is too small to be visible under SEM; however since they form bundles, it is possible to observe some of these bundles as seen at figure 3. The SEM images after the assembly show that there were some SWNT bundles inside the holes. They also stay partly on the surface since the length of SWNT is much larger than the array thickness.

Since SEM was not the most efficient technique to investigate how successful the assembly was, the current passing between the top and bottom layer of AAO, namely through the assembled SWNT was measured. Figure 4 shows the I–V curves of assembled SWNT as well as the control: alumina template without SWNT. This result was confirmed

by many repeated measurements with eight different samples. When there was no SWNT to provide electrical connection, no current was observed between top and bottom of the template.

On the other hand, I–V curve of assembled SWNT shows a Schottky diode type behavior. The SWNT used for assembly are a mixture of semiconducting and metallic types. Although the calculations showed the force on metallic ones are two orders of magnitude greater than semiconducting ones, because of the bundling of nanotubes, both types were assembled into the nanoholes. However the current passes preferentially on m-SWNT because they are the lower resistant path and also there is no applied gate voltage. Hence, it is expected to have a Schottky barrier between Si and m-SWNT.

I–V characteristics of a Schottky diode can be estimated by using the thermionic emission model [26]. The practical non-ideal diode is usually modeled as a series combination of a diode and a resistor, R. The forward current passing over the diode can be expressed as $I = I_S \exp[qV_D/nkT]$; where I_S depends only internal characteristics and effective area of the diode and temperature; q is the electronic charge, n is the ideality factor of diode, k Boltzmann constant, T is the absolute temperature and V_D is the voltage across the diode, $V_D = V - IR$. When the I–V curve of Au–SWNT–Si connection was fitted to thermionic emission model, the resistance is found as $R_{Au-SWNT-Si} = 17 \pm 3\ k\Omega$.

The area available for I–V measurement is the area sputtered with Au on AAO surface for electrical connection, which was 0.015 cm^2 for the chip. Hence, we achieved 2 mA cm^{-2} current density over assembled nanotubes per chip at 2 V bias, as seen in the inset of figure 4, which is same as the current density observed over nanotubes grown in AAO by a high temperature synthesis method [21].

However, the actual current density is much larger than 2 mA cm^{-2} since the electrical connection is through the SWNT which has much smaller diameter than the nanoholes. To have an approximation of the current density over the connection area, the effective area of assembly of the electrode setup was first estimated by low magnification SEM images of assembled beads. The SEM images showed that the radius of effective assembly site was 4 μm, which is smaller than the radius of the counter electrode (50 μm). The total effective assembly area for one chip was estimated as 50 sites $\times$ (circular area of assembly site) $= 50 \times \pi(4 \times 10^{-4})^2 \approx 2.5 \times 10^{-5}$ cm^2. From the SEM images of AAO, the average area of one nanohole is 1.6×10^3 nm^2. Several high-resolution SEM images, showing different cross-sections of the alumina template, were used to statistically determine the assembled nanotube per hole ratio, which was found to be 1.0 ± 0.3. Thus the number of assembled nanotubes is 1.6×10^6, by calculating the number of holes residing in the total effective assembly area. Since the total number of holes in the 0.32 cm^2 assembly area is approximately 2×10^{10}, the filling ratio of assembly area to total chip area can be estimated as 0.75/10 000. The total SWNT–Si connection area can be calculated by multiplying the number of assembled SWNT to the area of the one nanotube. Although the diameter of SWNT is known, their connection area cannot be calculated directly as they tend to form bundles. We have statistically extracted the average diameter of assembled nanotubes (3 ± 1 nm) from SEM images of the cross-sections of the alumina nanotemplate. Hence $A_{connection} = 1.6 \times 10^6 \pi (1.5 \times 10^{-7})^2 \approx (8.4 \pm 0.6) \times 10^{-7}$ cm^2. Therefore, the current density reaches 360 A cm^{-2} at 2 V bias when the estimated area of connection between SWNT and Si is used instead of total chip area. Interestingly, the current density of the connection between bulk aluminum and silicon reaches 30 mA cm^{-2} at 2 V bias (shown in figure 4(b)), which is $\sim$4 orders of magnitude lower than the estimated current density between SWNT and Si.

4. Conclusion

We demonstrated that SWNT can be assembled vertically into nanoporous holes by the combination of electrophoresis and dielectrophoresis. This method has many advantages such as mild condition assembly, post produced or commercially available SWNT utilization, high-rate and large scale assembly as well as integration of SWNT into existing Si platforms. It is also possible to attach AAO to Si after anodization in order to avoid exposure to acidic environments [27]. Using nanoscale features in the templates, we achieved large scale assembly of SWNT order of 10^6 elements over centimeter square areas. The strength of the connection established through these assembled SWNT is similar to the connection through in-grown nanotubes on Si. This assembly technique has potential applications of SWNT such as in CNT interconnects with the integration with Si microelectronics, in field emission displays or electronic memory devices.

Acknowledgments

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